ABSTRACT OF THE DISCLOSURE

~~Disclosed is here~~ a Memory Interface and Video Attribute Controller (MIVAC) ~~to be~~ inserted between a dynamic RAM (DRAM) capable of a consecutive data read operation, such as the operation associated with the static column mode, page mode, or nibble mode, and a graphic processor ~~achieving~~ to provide a parallel data processing. A serial data transfer is executed on each data bus between the MIVAC and the DRAM, whereas ~~a~~ parallel data transfer is conducted between the MIVAC and the graphic processor. As a result, the graphic processor can be configured with a reduced number of DRAMs so that the graphic processor operates without paying attention to the consecutive data read mode of the DRAM.